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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	Unknown
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	First Named Inventor	Alfredo Herrera
	Art Unit	Unknown
	Examiner	Unknown
Sheet 1 of 1	Attorney Docket No.	16550ROUS01U

U.S. PATENT DOCUMENTS				
Examiner's Initials	Citation Number	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document
	A1			
	A2			
	A3			

FOREIGN PATENT DOCUMENTS				
Examiner's Initials	Citation Number	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document
	B1			
	B2			

OTHER PRIOR ART -- NON-PATENT LITERATURE DOCUMENTS		
Examiner's Initials	Citation Number	Document Description -- Include the name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
	C1	*Field Programmable Gate Arrays An Enabling Technology*, (11 pages)
	C2	S. Lorenzini, *FPGA Design Cycle Time Reduction and Optimization*, (2 pages)
	C3	J. Ma, et al., *Incremental Design Techniques for Million-Gate FPGAs*, VTIP Disclosure No.: 01-110 (1 page)
	C4	*Xilinx Design Reuse Methodology for ASIC and FPGA Designers*, (27 pages)

Examiner Signature	VUTHE SIEK	Date Considered	4/15/06

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